

# TOOLSET FOR TEST AND VERIFICATION OF IP-BLOCKS WITH SPACEWIRE INTERFACE

**Session: SpaceWire Test and Verification**

**Short Paper**

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## **ABSTRACT**

Toolset for test and verification of RTL, post-synthesis and post-implementation models is usually based on BFM. The BFM (Base Formal Model) typically is used for testing and verification of interfaces that correspond to different standards. (Other term BFM – Base Functional Model is typically system level model of a particular device or IP-block). A toolset obligatory includes also generators of test sequences (or a prepared set of test sequences) and modules for monitoring and processing of test results. Often the toolset also includes an expanded set of components for simulation and performance estimation of the device in context of a real system. This expanded set could include switches, memory blocks and other devices.

We suggest to use this approach for SpaceWire toolset development. We specify the SpaceWire BFM as a multilayer structure, every layer of which corresponds to a layer of the SpaceWire standard. It allows to use the BFM for test and verification of SpaceWire controllers with support of different SpaceWire layers and at different stages of design. For example, if we plan to test IP-block, that includes layers from character to packet we will use only corresponding layers of a BFM in test shell. In many cases the detailed test of physical level is very important problem for SpaceWire product designers. BFM includes physical level also.

The important task of coordination between test tools and tested device or IP-block settings is considered.